REMARKS

Amendments of Claims 13, 15 and 17

Claims 13, 15 and 17 have been amended hereby to better delineate the invention described by the present application.

Specifically, claim 13 has been amended to recite <u>a double-gated/double-channel FIN MOSFET</u> having <u>vertical fin-shaped silicon-containing channel regions</u>. Support for the double-gated/double-channel FIN MOSFET can be found on page 1, line 13, page 2, lines 27-28, page 3, lines 21, 24-25, and page 4, line 24 of the instant specification as originally filed. Support for vertical fin-shaped silicon-containing channel regions can be found on page 1, line 10, page 2, lines 4-5, and page 9, line 30 of the instant specification as originally filed.

Claim 15 has been amended to depend from claim 14 instead of claim 13, since claim 14 contains the antecedent basis for "said insulating layer" and "said SOI material" recited by claim 15.

Claim 17 has been amended to clarify that the gate dielectric is a part of the insulating film recited in claim 16.

Response to the §102 Rejection of Claims 13-20

In the July 25, 2005 Office Action, the Examiner finalized the previous rejection of claims 13-20 under 35 USC §102(b) as being allegedly anticipated by U.S. Patent No. 5,963,800 to Augusto (hereinafter "Augusto").

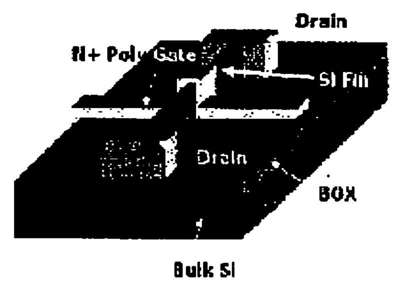
Applicants respectfully traverse the Examiner's rejections, for the following reasons:

Claim 13, from which claims 14-20 depend, has been hereby amended to positively recite <u>a double-gated/double-channel FIN MOSFET</u> that contains <u>vertical fin-shaped silicon-containing</u>

channel regions and a gate region that is self-aligned to the vertical fin-shaped silicon-containing channel regions.

It is well known in the art that the term "FIN" in the context of an FET structure refers to a thin *fin-shaped* body, which stands *vertically* on the substrate surface (i.e., the plane defined by this thin fin-shaped body is substantially perpendicular to the substrate surface) and functions as the channel region of the FET structure.

For example, the Semiconductor Glossary defines "FinFET" as an MOSFET that has a "fin"-like shaped body with the gate wrapped therearound (see http://semiconductorglossary.com/?searchterm=FinFET, as downloaded on September 13, 2005). Rahman, Design and Fabrication of Tri-Gated FinFET, 22[nd] Annual Microelectronic Engineering Conference (May 2004) shows an exemplary FinFET structure, which is reproduced at below for ease of reference:



In contrast, the MISFET device disclosed by the Augusto reference does not contain any vertical fin-shaped silicon-containing channel region, as positively recited by claims 13-20 of the present application. Augusto instead discloses a vertical MISFET device that has vertically arranged source, channel, and drain regions, for defining a current flow direction that is vertical to the substrate wafer (see Figure 5 of Augusto). However, nothing in Augusto teaches that the channel region of such a vertical MISFET device is a fin-shaped body that stands vertically on the substrate wafer. Therefore, the vertical MISFET device disclosed by Augusto does not constitute a FIN MOSFET within the meaning of claims 13-20 of the present application.

Further, nothing in the Augusto reference teaches either the use of a vertical fin-shaped silicon-containing channel or the construction of a FIN MOSFET device.

Applicants' claimed invention, as defined by the amended claims 13-20, thus patentably distinguishes over the Augusto reference, by positively reciting a double-gated/double-channel FIN MOSFET that contains vertical fin-shaped silicon-containing channel regions.

CONCLUSION

Based on the foregoing, claims 13-20 as amended herein are in condition for allowance. Issue of a Notice of Allowance for the application is therefore requested. If any issues remain outstanding, incident to the formal allowance of the application, the Examiner is requested to contact the undersigned attorney at (516) 742-4343 to discuss same, in order that this application may be allowed and passed to issue at an early date.

Respectfully submitted,

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Semiconductor Glossary

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Term (Index)	Definition
FinFET	innovative design of an MOSFET: built on SOI substrate on which silicon is etched into "fin"-like shaped body of the transistor, the gate is wrapped around and over the "fin" (double-gate structure).

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Design and Fabrication of Tri-Gated FinFET

Mohammed R.Rahman

Abstract- A Tri Gated Fin Field Effect Transistor is one of the many novel devices that may be replacing planar MOSFETs, by reducing short channel effects. The FinFET has emerged as one of the most promising double gate structures primarily because of its ease of manufacturing. There are still significant challenges to overcome it in order to make the process available commercially. The Tri-Gated FinFET is tri-gated meaning that the gate overlaps the top and the two sides of the FIN. Three dimensionally the gate depletes three surfaces of the FIN, which results in a higher drive current relative to a planar MOSFET. In order to reduce current crowding in the Fin corners, we have curved the corners using oxide etch back process. FinFETs has been built previously at Rochester Institute of Technology. We have designed and fabricated Tri-Gated FinFETs of various geometries. Electrical test showed poor performance of the devices. Proper scrutiny of the electrical results and the SEM micrographs allowed us to conclude that if LTO or Nitride is used as etch hard mask for silicon fin etch, electrical results closer to that of an ideal NMOS transistor could would be achieved.

Key Words: FinFET, MOSFET, SOI, Ion Implant, DIBL and Ballistic Transport.

of manufacturability using well-understood Planar MOS process steps.

1.2 Silicon-On-Insulator (SOI) Substrate

The figure 1 below shows the cross section of a SOI wafer.

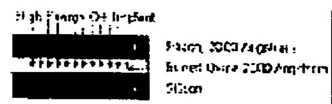

Figure 1. SOI Wafer

One of the most common ways to manufacture SOI wafers is by using SIMOX technology. The following process steps are done to make a SOI wafer [3].

- The starting material is typically a (100) device quality wafer. The wafer is first subjected to a high dose (~2 x $10^{18}cm^{-2}$) oxygen (O^+) ion implantation step at high enough energy (150-300KeV) so the peak (projected range) of the implant is deep within the silicon (0.3-0.5um). This step is usually carried out with the wafers held at >400 ^0C to ensure that the silicon maintains its crystallinity during the implantation.
- The wafers are given a post-implant anneal in N_2 for sufficient time (3-5 hours) at a relatively high temperature (1100-1175^0C). This step forms a buried oxide (BOX) layer of silicon dioxide near the peak of the implantation and removes any many of the defects (dislocations) formed during the ion implantation step. The depth of the ion

1 Introduction:

1.1 Need for FinFET

The scaling of planar MOS is approaching the practical limits. With the scaling of the channel length below 50nm, complex channel profiles are required to achieve desired threshold voltages and to eliminate short channel effects. Some of the proposed bulk structures for 50nm and beyond include Silicon on nothing (SON-planar ultra thin dual gate), Vertical MOS, Delta Doped MOSFET, etc. In all these structures, bulk doping concentration need to be increased to suppress the short channel effect this degrades mobility, worsens sub-threshold swing and increase parasitic junction capacitance [1]. Essentially, the short channel effect reflects the extent of drain-bias influence on channel potential. In order to increase gate control electrostatics, the entire channel semiconductor needs to be "brought closer to the gate" [1]. SOI (silicon on insulator) technologies such as Full-Depleted, Ground-plane and Double gate achieve this by using a thin silicon film controlled by one or more gates [1]. Researchers have shown through extensive Monte Carlo simulations that multi-gated structures are scalable to the lowest channel length for a given insulator thickness [2]. The FinFET is a dual or tri-gated structure that has become one of the most important choices for its ease

implantation defines the BOX depth and the BOX thickness is limited to about 0.5um.

- If additional Si thickness is required, an epitaxial Si layer can be grown to provide this additional thickness [3].

From the above process steps, it is seen that the BOX height is kept fairly low, and the reason for this is that the BOX is not a good thermal conductor. Thus the heat does not dissipate properly with thick BOX.

1.3 The FinFET

The figure 2 below shows the tilted 3-D cross section of the Fin-FET.

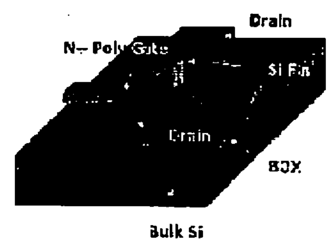

Figure 2 3D Tilted Cross Section of the FinFET [4]

Figure 2 above shows the 3D tilted cross section of the Fin-FET. The gate overlaps the fin from 3 sides. It is a type of Tri-gated MOSFET. The initial silicon doping before patterning is the same as the bulk substrate as shown above in the SOI manufacturing. Like

the conventional planar MOS the fin under the gate is essentially undoped. The rest of the silicon is doped with opposite polarity similar to a planar MOS. If the starting substrate were p-type 100 orientation SOI, the Fin and the source/drain would be doped with n-type dopants. The region under the gate would remain at the doping level of the starting material. At the assigned turn on gate voltage, channel would be formed in three faces of the fin, which further will define the FinFET state of operation. It has to be understood that three surfaces are getting inverted unlike single surface inversion of a planar MOSFET. The gate is high-doped n+polysilicon or insitu doped Si_xGe_y which will be discussed in the later sections. Our FinFet Gate metal was n+polysilicon

2 Theory

The FinFET is a symmetric three-gate structure. This means that both the front back and the top gates have the same work function and are tied to the same bias, so all the three surface channels are on at the same time. In this section the mathematical modeling of the symmetric double gate MOSFET FinFET Electrostatics are first explained which is followed by the Design theory Scaling effects. Mathematical modeling for a tri-gated FinFET is still under investigation and no journal has been published. It will be similar to that of a DG-FinFET and the only difference will be the addition of a top transistor to the DGFinFET modeling results. The modeling of the top gate in the first order will just be an addition of a transistor, which is the same as a planar MOSFET, with the width of the Fin defining the width of the planar MOSFET. Thus for simplicity, we derive the current equations for a DG-FinFET in the next subsection.

$$I_{DS} = \mu_{eff} W q_1 \frac{dV_{ch}}{dy}$$

where q_1 is the normalized inversion layer charge given by $Q_{inv}/C_{ox}\phi$. V_{ch} is the quasi Fermi potential in the channel and the current flows in the positive y direction. The inversion charge in the channel can also be expressed by

$$q_i(y) = q_{i0} \exp\left[\left(\phi_s(y) - V_{ch}(y)\right) / V_{th}\right]$$

where Vth is the same as ϕ_t or kT/q.

In the original modeling of reference 5 the two gates were considered to be asymmetric and thus to account for that an ideality factor of n was used. For the case of the FinFET the n_i term can be reduced to equation (3) as shown below.

2.1 Mathematical Modeling of the FinFET.

Reference [5] describes initial framework of the FinFET model with given constraints and the results are applicable for any kind of double gate MOSFET. For simplicity, the important results are written in the paper. I have modified a number of equations of reference 5 for simplifying the models to only symmetric Double Gate FinFET structure. Figure 3b [ref 5] shows the 3D view of the FinFET showing only the silicon Fin and the two gates and figure 3b is a top down schematic.

Figure 3a. FinFET
Schematic of the FinFET.

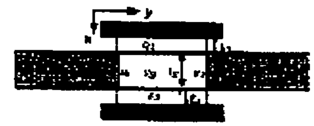

Figure 3b 2D Top Down

In the modeling, current for the two interfaces are calculated separately and added together. W or the width is the height of the FinFET. The vertical charge distribution provides a weigh to form a weighted sum of the contribution from the 2 currents at the 2 surfaces [5]

The drain current along of the surfaces is given by

$$n_1 = 1 + \left(\frac{C_{si}}{C_{si} - C_{OX}}\right) \qquad (3)$$

An expression for current in terms of charge is obtained as

$$I_{DS} = \mu_{eff} W \frac{(1 + q_i/n_1) dq_i}{dy} \qquad (4)$$

Integrating (2) from source to drain, the drain current is explicitly given by

$$I_{DS} = \frac{\mu_{eff} W}{L}\left[\frac{q_s^2 - q_d^2}{2n_1} - (q_s - q_d)\right] \qquad (5)$$

where q_s and q_d are the normalized charge at the source and drain respectively. The author has modified equation (10) of reference 5 to get the analytical solution for q_i. Equation 6 below is an analytical solution for q_i.

$$q_s = a\ \ln\left[\frac{\eta V_G - V_T}{n_1} - V_{ch}\right] \qquad (6)$$

In order to solve for the q_s and q_d, the V_{ch} has to be replaced by the source and the drain voltage respectively. V_T is the threshold voltage, which is given by equation (7) below.

$$V_T = 2V_{ox} + 2\phi_s + qN_a t_{si}\left(\frac{C_s - C_{ox}}{C_s C_{ox}}\right) \qquad (7)$$

In equation (7) t_{si} is the width of the Fin and ϕ_F is the fermi potential. It can be seen that the C_{ox} and C_s are in series.

2.2 Design Theory and Dimensions:
Fin Height (I):

The height (h) of the FIN represents the channel width of a single-fin transistor as illustrated in figure 2. The current I_{DS} for conventional and FinFET transistor technologies (I_{DS} = current per unit channel width) is proportional to the channel width as shown in equation 5. Thus for a single-fin FinFET would be proportional to

→ $I_{DS} \propto (2 \times h) = W_{FET}$ (α is the sign of proportionality) (10)

Where 'h' is the height of the fin and the width of the side channels. If more fins are placed the right side of equation has to be multiplied by the number of FINs. The equation becomes

$I_{DS} \propto [(2 \times h)] \times n_{fin}$ (n_{fin} is the number of Fins) → $n_{fin} W_{FET}$ (11)

From the above equation it can be seen that increasing the number of FINs can increase the drive current.

If multiple FINs are used, the following condition has to be used

2 X h ≥ pitch (12)

This is a small sub section, which talks about the design rules of the FinFET design. The design rule details are presented in reference 1. In this section the design rules are summarized from reference 1.

Fin Thickness (I):

As channel length decreases, fin thickness and oxide thickness must be decreased to maintain gate control. In accordance with scaling rules based on natural length [1] the following design rule will have be followed

→ 0.7 x Length of Fin under Gate ≥ Fin Thickness (8)

→ 0.3 x Fin Thickness ≥ Thickness of Gate Oxide (9)

Where pitch is the horizontal gap between two fins.

Source/Drain Resistance:

Source/Drain extension resistance is a significant component of parasitic series resistance. The cross sectional area of the source/drain extensions is determined by the FIN thickness [1]. Common methods of reducing source/drain series resistance is by raising the S/D, extra doping of fin area excluding the area under the gate and silicidation of source/drain contact.

3. Designs and Fabrication:

FinFETs of various geometries were designed. The smallest device had a Fin Width of 0.5um and Gate Width of 0.6um. FinFETs of other geometries were also included in the mask. FETs with multiple fins were also included. Below are fabrication process steps listed in sequence starting from Level 1 the Alignment Level

1 Starting Substrate 100 P-type silicon wafer with BOX thickness of 2300 and Silicon thickness of 3750.

2 Lithography Level 1: Alignment Marks Patterning.

3 Alignment marks were patterned, and finally etching the 3750A silicon using reactive ion etching transferred the image and the 2300A BOX using buffered oxide etching.

4 Lithography Level 2: Source/Drain FIN Patterning

5 After the Level 2 was patterned, the silicon Fin, source and drain, masked by OCG 82C positive photoresist were etched down to BOX, using DryTech Quad Reactive Ion Etching. In order to etch the silicon completely in the unmasked area, the following etch recipe had to be used

RF Forward: 185 Watts
Pressure: [illegible] mTorr
SF_6: [illegible] SCCMs
CHF_3: 18 SCCMs
Etch Time: 145 Minutes

Different pattern density mask was used while doing the process development of this recipe, but due to severe micro loading effect, the etch time was very different from the target etch time.

6 Resist Ash in Branson Asher.

7. After the Resist ash was done, a sacrificial SiO_2 of thickness one 160Angstrom was grown. The Sacrificial Oxide was then etched away using Hydrofluoric Acid Chemistry. This step was done for two reasons. Firstly for rounding the corners for the Fin/Fins so that current crowding or spreading resistance effects can be prevented. The next reason was to prepare the surface for the gate oxide

8. Gate oxide of 580Angstrom was grown using the Bruce Dry Oxide Furnace. For the prevention of Fixed Charges, nitrogen annealing was done after growth step.

5. Poly Silicon of thickness 2300Angstrom was deposited using Low Pressure Chemical Vapor Deposition.

10. Level 3 Lithography: Gate Patterning

11. After the gate was patterned the polysilicon in the unmasked area was etched using the Dry Tech Quad Reactive Ion Etcher Etcher. The etch recipe was as follows:

RF Forward Power: 135Watts
SF_6: 30SCCMs
CHF_3: 30 SCCMs
Pressure: 43mTorr
Etch Time: 2minute 10seconds.
12. Resist Ashing in Branson Asher was done using oxygen plasma.

13. Ion Implantation for Self-Aligned Source/Drain and Gate:

Ion-Implant of phosphorus using the Varian 350D ion-implanter was done to introduce dopants into the polysilicon, gate and source/drain. In order, to prevent channeling and implant damage the implant in the Source/Drain are was done through the 500Angstrom dry oxide. The implant conditions were as follows

Implant Specie: P31
Implant Energy: 60KeV
Implant Dose: $1 \times 10^{15}/cm^2$

14. Activation of the Dopant Ions

Annealing the wafer at 1000°C for 15minutes in the furnace activated dopant ions.

15. Oxide Etch

Oxide in the Source/Drain area etched using Hydrofluoric Acid base etchant.

16.Aluminum Deposition

The source/drain contact area was slightly bigger than the probe contact are. Thus a separate contact mask was not used. To make an ohmic contact with the source/drain 2000 Angstrom of aluminum was deposited by evaporation using the CVC evaporator. The base pressure of the evaporation process was 4.2×10^{-6} Torr.

17. Level 4 Lithography: Metal Patterning

Aluminum in the Source/Drain and Polysilicon contact area were masked using photoresist.

18. Aluminum Etch:

Wet Aluminum Etch was done in the unmasked areas using phosphoric acid based chemistry. The etch time was 47seconds, which includes a 100% over etch.

19: Sintering

To make the contact ohmic, the wafer was sintered in the furnace at 450°C in Forming Gas ambient.

4. Electrical Results and Analysis:

Electrical tests were done using the Keithly 4200 Semiconductor Parameter Analyzer. The electrical results showed very poor performance. Figure 4 below shows the drain family of curves for one of the FinFETs.

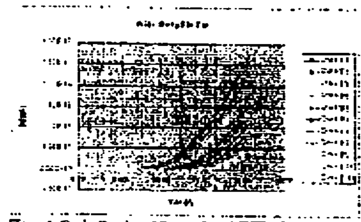

Figure4: Drain Family of Curve for a NFET FinFET.

A proper scrutiny of figure 4 shows that, current flows only had very high Vds. The current flow decreases as the gate bias is increased. All the other transistors showed similar performance. In order to further investigate the results, we took high magnification scanning electron micrographs of the devices. Figure 5 shows the SEM micrographs.

Mohammed Rahman

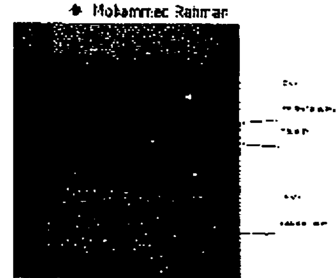

Figure 5a: FinFET of 0.5 gate length and 4um Fin

Figure 5b: FinFET of 0.5 gate length and 0.8um Fin

Investigation of the electrical results show that there were large pits and holes in the silicon fin and the source drain areas. This pit and holes came from the second level etch, that is the etch of the Source/Drain and Fin as described in the process flow. The pits and the holes pattern got transferred in the other levels. Another FinFET project was conducted with my project [5], which used low temperature oxide as a hard mask to etch the silicon Fin. A SEM micrograph of the other project using LTO as a hard mask after the Source/Drain and Fin etch is shown in figure 6.

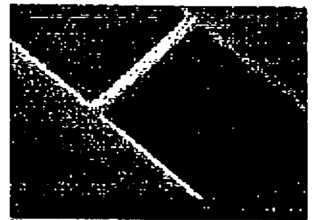

Figure 6: 0.5um FinFET reference [6]

Figure 7 below show the electrical results of the second groups' device:

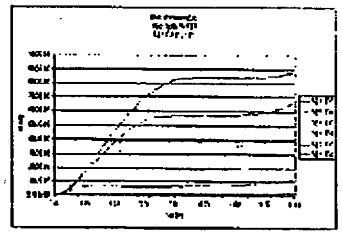

Figure 7: Electrical Result of FinFET [6]

After investigating and analyzing the results we can say that photo resist alone is not a sufficient etch mask. The other group's FinFET works because it is protected by a separate hard etch mask. The Roughness caused holes and voids to be formed through the box. The roughness also transferred to the Polysilicon Gate. As a result the fin was highly resistive and the metal short-circuited with the silicon under the BOX. This caused Current Flow from under the Box at high Vds. Further Field Effect due to increasing Vgs reduced the current flowing under the gate.

5. Conclusion:

Cb620 Resist is not sufficient to mask the silicon etch due to its poor selectivity. This results in highly resistive Fin. We learned that a hard mask like LTO or silicon nitride has to be used for the silicon fin Etch.

6 Acknowledgements :

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